

(19) World Intellectual Property Organization
International Bureau



(43) International Publication Date
6 September 2002 (06.09.2002)

PCT

(10) International Publication Number
WO 02/069047 A1

(51) International Patent Classification⁷: **G03F 7/20**, 9/00

Wilder Mann Str. 43, 01129 Dresden (DE). **SCHMIDT, Sebastian** [DE/DE]; Moritzburgerstr. 28, 01127 Dresden (DE). **FISCHER, Thomas** [DE/DE]; Meisensteig 9, 01109 Dresden (DE).

(21) International Application Number: PCT/EP02/02029

(22) International Filing Date: 25 February 2002 (25.02.2002)

(74) Agent: **EPPING, HERMANN & FISCHER**; Ridlerstr. 55, 80339 München (DE).

(25) Filing Language: English

(26) Publication Language: English

(81) Designated States (*national*): JP, KR, US.

(30) Priority Data:
01104358.5 23 February 2001 (23.02.2001) EP

(84) Designated States (*regional*): European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE, TR).

(71) Applicant (*for all designated States except US*): **INFL-NEON TECHNOLOGIES AG** [DE/DE]; St.-Martin-Str. 53, 81669 München (DE).

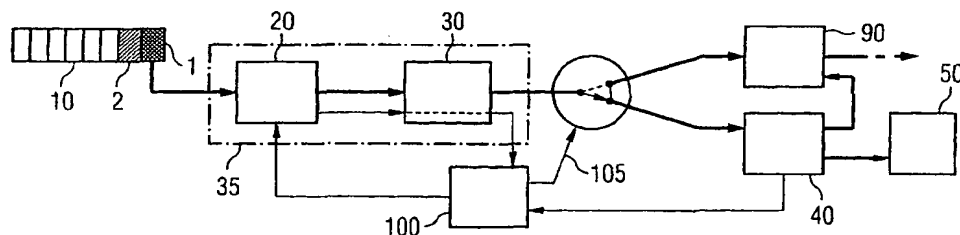
Published:
— with international search report
— before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments

(72) Inventors; and

(75) Inventors/Applicants (*for US only*): **HOMMEN, Heiko** [DE/DE]; Böhmische Str. 15, 01099 Dresden (DE). **OTTO, Ralf** [DE/DE]; Zu den Kleingärten 35, 01723 Kesselsdorf (DE). **SCHADEL, Thorsten** [DE/DE];

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

(54) Title: METHOD FOR EXPOSING AT LEAST ONE OR AT LEAST TWO SEMICONDUCTOR WAFERS



(57) Abstract: Semiconductor wafers (1, 2), e.g. a lot (10), are exposed after an alignment (20) in a wafer stepper or scanner (35) with each determining their alignment parameters. Using, e.g., a linear formula with tool specific coefficients the overlay accuracy can be calculated from these alignment parameters in advance to a high degree of accuracy as if a measurement with an overlay inspection tool (40) had been performed. The exposure tool-offset can be adjusted on a wafer-to-wafer basis to correct for the overlay inaccuracy derived. Moreover, the alignment parameters for a specific wafer can be used to change the tool-offset for the same wafer prior to exposure. The required inspection tool (40) capacity is advantageously reduced, the wafer rework decreases and time is saved to perform the exposure step (30).